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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/822,826	04/13/2004	Youichi Tobita	251786US2	4801

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EXAMINER	
TRA, ANH QUAN	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/822,826	TOBITA, YOUICHI	
	Examiner	Art Unit	
	Quan Tra	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) *7-14* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/13/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group 1, claims 1-6 in the reply filed on 07/05/05 is acknowledged.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-4 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Kim et al. (US 2002/0122324).

As to claim 1, Kim et al.'s figure 7 a voltage generating circuit comprising: a first transistor (the second upper NMOS on the left) of a first conductivity type (N-type) connected between a reference voltage node supplied with a predetermined voltage (Vdd) and a first internal node, and having a control electrode connected to a second internal node; a second transistor (the second lower NMOS on the left) of the first conductivity type connected between the reference voltage node and the second internal node, and having a control electrode connected to said first internal node; a first capacitance element (the most left upper capacitor or capacitor CP1 in figure 5) a connected between a first input node receiving a first control signal (CLK3) controlling a precharging operation and the first internal node; a second capacitance element (the lower capacitor) connected between a second input node receiving a second control signal (CLK1) controlling charge accumulation and the second internal node; a third transistor

(the PMOS connected to the first capacitance or transistor TP1 in figure 5) of a second conductivity type connected between the second internal node and an output node, and having a control electrode connected to a third internal node; a third capacitance element (capacitor connected to the gate of the third transistor or capacitor CP1 in figure 5) connected between the third internal node and a third input node receiving a third control signal (CLK4) controlling charge transfer; and a fourth transistor (transistor MPB1) of the second conductivity type connected between the output node and the third internal node, and having a control electrode connected to the second internal node.

As to claim 2, figure 7 shows at least one voltage drive stage connected between the output node and a final output node, for generating a final voltage on the final output node, the voltage drive stage including; a fifth transistor (PT2) of the second conductivity type connected between an input node of the voltage drive stage and an output node of the voltage drive stage, and having a control electrode connected to a fourth internal node, a fourth capacitance element (CP2) coupled to the input node of the voltage drive stage, the first and second control signals being applied alternately to the fourth capacitance elements in a connection sequence when the at least one voltage drive stage includes a plurality of such voltage drive stages, a sixth transistor (MPB2) of the second conductivity type connected between the fourth internal node and the output node of said voltage drive stage, and having a control electrode connected to the input node of the voltage drive stage, and a fifth capacitance element (CB2) coupled to the fourth internal node, a fourth control signal and the third control signal being applied alternately to the fifth capacitance elements in the connection sequence when the at least one voltage drive stage includes a plurality of such voltage drive stages.

As to claim 3, figure 6 shows that the second control signal attains a first logical level when a predetermined time elapses since the first control signal changes from the first logical level to a second logical level, and changes from the first logical level to the second logical level before the first control signal changes from the second logical level to said first logical level, the third control signal changes from the first logical level to the second logical level when a predetermined time elapses since the second control signal changes to the first logical level, and changes from the second logical level to the first logical level before the second control signal changes from the first logical level to the second logical level, the third control signal changes from the first logical level to the second logical level when a predetermined time elapses since the second control signal changes to the first logical level, and changes from the second logical level to the first logical level before the second control signal changes from the first logical level to the second logical level, and the fourth control signal is set at the second logical level for a predetermined time period when the first control signal is at the first logical level and the second control signal is at the second logical level, before the first control signal changes to the second logic level after elapse of a predetermined time since transition of the second control signal to the second logic level.

As to claim 4, figure 7 shows that the at least one voltage drive stage includes a plurality of cascaded voltage drive stages.

As to claim 6, figure 7 shows that output node generates an internal voltage applied to internal circuitry, and said voltage generating circuit further includes a capacitance element connected to said output node.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kim et al. (US 2002/0122324) in view of Lin et al. (6642773).

Kim et al.'s figure 7 shows all elements of claim except a capacitance element connected to the final output node. However, Line et al.'s figure 3 shows a charge pump having a capacitor (62) coupled to the final output for stabilizing the output voltage. Therefore, it would have been obvious to one having ordinary skill in the art to add a capacitor coupled to Kim et al.'s final output node for the purpose of stabilizing the output node.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Quan Tra whose telephone number is 571-272-1755. The examiner can normally be reached on 8:00 A.M.-5:00 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QUAN TRA
PRIMARY EXAMINER
ART UNIT 2816

August 8, 2005